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INVENTORS DESIGNATION SHEET

TITLE: SEMICONDUCTOR DEVICE WITH A MULTI-LEVEL INTERCONNECT STRUCTURE AND METHOD FOR MAKING THE SAME

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SEMICONDUCTOR DEVICE WITH A MULTI-LEVEL INTERCONNECT STRUCTURE AND METHOD FOR MAKING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of Taiwanese Patent Application No. 091134054, filed on November 22, 2002.

BACKGROUND OF THE INVENTION

1. Field of the invention

This invention relates to a semiconductor device, and more particularly to a semiconductor device with a multi-level interconnect structure and to a method for making the same.

2. Description of the related art

With the increase of functions in a highly integrated semiconductor chip and with the decrease in the size of the semiconductor chip, not only the distance between adjacent bonding pads formed on the semiconductor chip is getting smaller. However, electrical contacts on an external electronic device, especially, a wiring substrate, and the distance between adjacent electrical contacts, are unable to be as small as the bonding pads on the semiconductor chip. As a consequence, connecting the bonding pads formed on the semiconductor chip to the electrical contacts formed on the external electronic devices through solder bumps becomes very difficult, and short circuit tends to occur, which leads to lower production yield.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a semiconductor device that is capable of overcoming the aforesaid drawback of the prior art.

Another object of the present invention is to provide a method for making the semiconductor device.

According to one aspect of the present invention, there is provided a semiconductor device that comprises: a semiconductor die having a pad-mounting surface defining a horizontal plane, and a plurality of spaced apart bonding pads formed on the pad-mounting surface; and a multi-level interconnect structure formed on the pad-mounting surface. The multi-level interconnect structure includes: a first insulating layer formed on the pad-mounting surface and formed with a plurality of holes, each of which exposes a respective one of the bonding pads from the pad-mounting surface; a plurality of first level conductive horizontal bodies, each of which has an end section that fills a respective one of the holes to electrically connect with a respective one of the bonding pads, and an extension that extends from the end section, that is formed on the first insulating layer, and that has a connecting end horizontally offset from the respective one of the holes; a second insulating layer formed on the first insulating layer and formed with a plurality of holes, each of which

exposes the connecting end of the extension of a respective one of the first level conductive horizontal bodies from the second insulating layer; and a plurality of second level conductive vertical bodies, each of which fills a respective one of the holes in the second insulating layer to electrically connect with the connecting end of the extension of a respective one of the first level conductive horizontal bodies, and each of which has a connecting end that extends through the respective one of the holes in the second insulating layer.

According to another aspect of the present invention, there is provided a method for making a semiconductor device that includes a semiconductor die having a pad-mounting surface defining a horizontal plane and a plurality of bonding pads formed on the pad-mounting surface. The method comprises the steps of: forming a first insulating layer on the pad-mounting surface; forming a plurality of holes in the first insulating layer, each of the holes exposing a respective one of the bonding pads from the first insulating layer; forming a plurality of first level conductive horizontal bodies, each of which has an end section that fills a respective one of the holes to electrically connect with a respective one of the bonding pads, and an extension that extends from the end section, that is

formed on the first insulating layer, and that has a connecting end horizontally offset from the respective one of the holes; forming a second insulating layer on the first insulating layer; forming a plurality of holes in the second insulating layer, each of the holes in the second insulating layer exposing the connecting end of the extension of a respective one of the first level conductive horizontal bodies; and forming a plurality of second level conductive vertical bodies, each of which is electrically connected to the connecting end of the extension of a respective one of the first level conductive horizontal bodies, each of which fills a respective one of the holes in the second insulating layer, and each of which has a connecting end that extends through the respective one of the holes in the second insulating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

In drawings which illustrate an embodiment of the invention,

Fig. 1 is a schematic view to illustrate how a first insulating layer is formed on a semiconductor die of the preferred embodiment of a semiconductor device according to the method of this invention;

Fig. 2 is a schematic view to illustrate how holes are formed in the first insulating layer according to the method of this invention;

Figs. 3 and 4 are schematic views to illustrate how first level conductive horizontal and vertical bodies are formed on the first insulating layer according to the method of this invention;

Fig. 5 is a schematic view to illustrate how a second insulating layer is formed on the first insulating layer according to the method of this invention;

Fig. 6 is a schematic view to illustrate how second level conductive horizontal and vertical bodies are formed on the second insulating layer according to the method of this invention;

Fig. 7 is a schematic view to illustrate how a third insulating layer is formed on the second insulating layer according to the method of this invention; and

Fig. 8 is a schematic view to illustrate how conductive bumps are formed on the second level conductive horizontal and vertical bodies according to the method of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figs. 1 to 8 illustrate consecutive steps of forming the preferred embodiment of a semiconductor device according to the method of this invention. The semiconductor device includes a semiconductor die 1 having a pad-mounting surface 10 and a plurality of spaced apart first and second bonding pads 11, 12 (see

Fig. 3) formed on the pad-mounting surface 10, and a multi-level interconnect structure which is formed according to the following steps of the method of this invention. Note that the semiconductor die 1 can be replaced with a semiconductor wafer.

The method includes the steps of: forming a first insulating layer 2 of a photoresist material on the pad-mounting surface 10 (see Fig. 1); forming a plurality of first and second holes 13 in the first insulating layer 2 through etching techniques (only one of the first and second holes 13 is shown in Fig. 2), each of the first and second holes 13 exposing a respective one of the first and second bonding pads 11, 12 from the first insulating layer 2; forming a plurality of first metal layers 41 on the first bonding pads 11, respectively, through plating techniques; forming a plurality of first level conductive horizontal bodies 3 (see Figs. 3 and 4), each of which has an end section 31 that fills a respective one of the first holes 13 to electrically connect with a respective one of the first bonding pads 11 through a respective first metal layer 41, and an extension 32 that extends from the end section 31; that is formed on the first insulating layer 2, and that has a connecting end 320 horizontally offset from the respective one of the first holes 13, each of the first level conductive horizontal bodies 3

including a conductive paste layer 42 that has a first portion extending from the first metal layer 41, and a second portion formed on the first insulating layer 2, and a second metal layer 43 formed on and cooperating with the second portion of the conductive paste layer 42 to define the extension 32 of the respective one of the first level conductive horizontal bodies 3, the connecting end 320 of the extension 32 of each of the first level conductive horizontal bodies 3 being flattened, the second metal layer 42 preferably including a nickel sub-layer and a gold sub-layer (not shown); forming a plurality of first level conductive vertical bodies 3', each of which fills a respective one of the second holes 13 in the first insulating layer 2 to electrically connect with a respective one of the second bonding pads 12 (see Figs. 3 and 4), and each of which has a connecting end 31' that extends through the respective one of the second holes 13 in the first insulating layer 2; forming a second insulating layer 5 of the photoresist material on the first insulating layer 2 (see Fig. 5); forming a plurality of first and second holes 50 in the second insulating layer 5 (see Fig. 5), each of the first holes 50 in the second insulating layer 5 exposing the connecting end 320 of the extension 32 of a respective one of the first level conductive horizontal bodies 3, each of the

second holes 50 in the second insulating layer 5 exposing the connecting end 31' of a respective one of the first level conductive vertical bodies 3'; forming a plurality of second level conductive vertical bodies 6 (see Fig. 6), each of which is electrically connected to the connecting end 320 of the extension 32 of a respective one of the first level conductive horizontal bodies 3, each of which fills a respective one of the first holes 50 in the second insulating layer 5, and each of which has a connecting end 60 that extends through and that is vertically aligned with the respective one of the first holes 50 in the second insulating layer 5; forming a plurality of second level conductive horizontal bodies 6' (see Fig. 6), each of which has an end section 60' that fills a respective one of the second holes 50 in the second insulating layer 5 to electrically connect with the connecting end 31' of a respective one of the first level conductive vertical bodies 3', and an extension 61' that extends from the end section 60' of a respective one of the second level conductive horizontal bodies 6', that is formed on the second insulating layer 5, and that has a connecting end 611' horizontally offset from the respective one of the second holes 50 in the second insulating layer 5, the connecting end 611' of the extension 61' of each of the second level conductive

horizontal bodies 6' being flattened; forming a third insulating layer 7 of the photoresist material on the second insulating layer 5 (see Fig. 7); forming a plurality of first and second holes 70 in the third insulating layer 7 (see Fig. 7) such that the connecting end 60 of each of the second level conductive vertical bodies 6 and the connecting end 611' of the extension 61' of each of the second level conductive horizontal bodies 6' extend into a respective one of the first and second holes 70 in the third insulating layer 7; forming a third metal layer 8 on the connecting end 60 of each of the second level conductive vertical bodies 6 and on the connecting end 611' of the extension 61' of each of the second level conductive horizontal bodies 6' (see Fig. 7); and forming a plurality of first and second conductive bumps 9, 9' (see Fig. 8) such that each of the first conductive bumps 9 extends into a respective one of the first holes 70 in the third insulating layer 7 to electrically connect with the connecting end 60 of a respective one of the second level conductive vertical bodies 6 through the third metal layer 8, and that each of the second conductive bumps 9' extends into a respective one of the second holes 70 in the third insulating layer 7 to electrically connect with the connecting end 611' of the extension 61 of a respective one of the second

level conductive horizontal bodies 6' through the third metal layer 8. Note that the multi-level interconnect structure is not limited to the above preferred embodiment, and can include more levels of the insulating layers and the conductive horizontal and vertical bodies.

With the formation of the multi-level interconnect structure on the semiconductor die 1, connection of external electronic devices (not shown) to the bonding pads 11 of the semiconductor die 1 can be shifted to the first and second conductive bumps 9, 9', which are wider in distance between adjacent ones as compared to the bonding pads 11. As such, the aforementioned drawback as encountered in the prior art can be eliminated.

With the invention thus explained, it is apparent that various modifications and variations can be made without departing from the spirit of the present invention. It is therefore intended that the invention be limited only as recited in the appended claims.